REMARKS

Amendments to Specification

Paragraph [0058] of the Specification is amended herein to update the reference in the paragraph to state "U.S. Patent Application No. 10/602,991, titled 'Erase Block Data Splitting', filed June 24, 2003, and which issued on June 14, 2005 as U.S. Patent No. 6,906,961." Applicant respectfully contends that no new matter has been added by the correction of these typographical errors.

Applicant therefore respectfully requests that the Examiner approve the amendments to the Specification.

Claim Rejections Under 35 U.S.C. § 112

Claims 46-62 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such as way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant respectfully traverses the rejection.

The Examiner stated, in regard to claims 46-62, that "[c]laims 46-62 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 46 and 54 incorporate the language reading one or more user data sectors and/or ECC codes and writing the one or more user data sectors and/or ECC codes. The Examiner was not able to find any description in the specification to enable the and/or *(sic)* claimed features. Clarification is required."

Applicant is unsure of which features recited in claims 46-62 the Examiner is asserting as not being described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. Applicant therefore respectfully requests that the Examiner further detail as to which features the Examiner is specifically asserting as not being enabled by the Specification. In addition, Applicant also notes that the elements of language reading one or more user data sectors and/or ECC codes and writing the one or more user data sectors and/or ECC codes is detailed, at least, in Figures 3A-3B and 5A-5B and at Paragraphs [0042]-[0050] and [0065]-[0070] of the Specification of the Present Application.

Applicant respectfully maintains that claim 46 recites, in part, a "non-split data move control circuit is adapted to read one or more user data sectors and/or ECC codes of a source physical row page of a source erase block of a NAND architecture Flash memory device and write the one or more user data sectors and/or ECC codes to a target physical row page of a target erase block addressed by the target row register, where the non-split data move control circuit is adapted to transfer the one or more user data sectors and/or ECC codes from the NAND architecture Flash memory device, and where the non-split data move control circuit is adapted to mask a selected range of read data as it is held in a data latch." Applicant respectfully maintains that this is supported, at least, by Figure 3A, and Paragraphs [0042] and [0044]-[0045] of the Present Application. In particular, Paragraph [0044] states "[i]n a NAND architecture Flash memory embodiment of the present invention, a data move operation moves the selected logical data sector(s) and overhead/ECC data areas 314 from the source row page 310 to the target row page 312 utilizing a modified copy-back operation." Applicant thus contends that relevant features of claim 46 are supported and described in the specification so as to enable one skilled in the art to practice the invention.

Claim 54, recites, in part, a "split data move control circuit is adapted to read one or more user data sectors and/or ECC codes of a source A physical row page of a first erase block of a source erase block pair and write the one or more user data sectors and/or ECC codes to a target A physical row page of a first erase block of a target erase block pair addressed by the target A row register, and read one or more user data sectors and/or ECC codes from a source B physical row page of a second erase block of the source erase block pair and write the one or more user data sectors and/or ECC codes to a target B physical row page of a second erase block of the target erase block pair addressed by the target B row register." Applicant respectfully maintains that claim 54 recites the reading one or more user data sectors and/or ECC codes and writing the one or more user data sectors and/or ECC codes in a split data memory and that this is supported, at least, by Figures 3B, 4, and 5A-5B; and Paragraphs [0046]-[0050] and [0058]-[0069]. In particular, Paragraph [0046] states "Figure 3B details a split data move operation with a corresponding sequential pair of data split Flash memory physical row pages 350, 352 of a NAND architecture Flash memory device array of an embodiment of the present invention. During the move a selected set of logical sectors 358 and associated overhead data/ECC areas 360 are moved from the source pair of data split Flash memory physical row pages 350, 352 to a target sequential pair of data split Flash memory physical row pages 354, 356." Applicant thus

contends that relevant features of claim 54 are supported and described in the specification so as to enable one skilled in the art to practice the invention.

Applicant respectfully contends that claims 46 and 54 have been shown to be supported by the specification and that the specification does clearly describe the invention in a way to enable one skilled in the art to make or use the invention. As claims 47-53 and 55-62 depend from and further define claims 46 and 54, respectively, they are also believed to be enabled. Applicant therefore respectfully requests that the rejection of claims 46-62 under 35 U.S.C. § 112, first paragraph, be withdrawn in that the claims are supported by the specification and that the specification does clearly describe the invention in a way to enable one skilled in the art to make or use the invention.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-6, 29-32, 38-40, 44, 67, 69-70, 73-74, 85-88, 93-95, 98 and 101 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Estakhri et al. (U.S. Patent No. 6,262,918) in view of Iwata et al. (U.S. Published Application No. 2004/0193774) and Harper III, et al.(U.S. Patent No. 4,918,600). Claims 7, 33 and 41 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Estakhri et al. (U.S. Patent No. 6,262,918) in view of Iwata et al. (U.S. Published Application No. 2004/0193774) and Harper III, et al. (U.S. Patent No. 4,918,600) as applied to claim 1 above and further in view of Miura et al. (U.S. Published Application No. 2006/0041711). Claims 8-9, 11-14, 16-17, 20-21, 25-26, 36, 45, 75-76, 78, 84, 89-92 and 102 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Estakhri et al. (U.S. Patent No. 6,262,918) in view of Iwata et al. (U.S. Published Application No. 2004/0193774) and Gonzalez et al. (U.S. Patent No. 7,032,065). Claims 15, 19, 27 and 79 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Estakhri et al. (U.S. Patent No. 6,262,918) in view of Iwata et al. (U.S. Published Application No. 2004/0193774) and Gonzalez et al. (U.S. Patent No. 7,032,065) as applied to claim 8 above and further in view of Miura et al. (U.S. Published Application No. 2006/0041711). Applicant respectfully traverses these rejections and submits that claims 1-9, 11-17, 19-21, 25-27, 29-33, 36, 38-41, 44-45, 67, 69-70, 73-76, 78-79, 84-95, 98 and 101-102, as pending, are allowable for at least the following reasons.

Applicant respectfully maintains that Estakhri et al. discloses a parallel erasing Flash memory system that groups an erase block from each Flash memory device in the system into a "super block" and erases them in parallel, reducing the overall erase time from that of serially erasing the same number of erase blocks from a single Flash memory device. *See, e.g.*, Estakhri

et al., Figure 2; Column 2, line 62 to Column 3 Line 54; and Column 9, Line 7 to Column 10, Line 23.

Applicant notes that the Specification of the Present Application defines a split data non-volatile memory devices or systems as having split user/overhead data that avoids the issue of potential corruption of both the user data and overhead data due to each being held within close proximity to each other or on the same physical row (wordline), and super blocks as pairs of erase blocks where when user data is read from a sector of an erase block of the Flash memory 200, the overhead data for the user data is read from the overhead data area of a sector of the associated erase block of the erase block super block pair. *See*, Paragraphs [0010], [0025], [0035] and [0038] of the Specification of the Present Application.

Applicant therefore submits that Estakhri et al does not teach or suggest a split data non-volatile memory device or system that has split user/overhead data wherein the user data and overhead data of a given sector are not stored within close proximity to each other or on the same physical row (wordline) or super blocks, wherein each super block contains a pair of erase blocks where user data is read from a sector of an erase block of the super block, the overhead data for the user data is read from the overhead data area of a sector of the associated erase block of the erase block super block pair. As such, Applicant submits that Estakhri et al. does not teach or suggest each and every element of the Applicant's claimed invention.

Applicant respectfully maintains that Iwata et al. discloses a Flash memory card that has a Flash controller with an erase block data merge circuit which operates to consolidate data to a new erase block from an old erase block and subsequent erasure of the old erase block. Applicant maintains that, in disclosing a data merge circuit and operation, Iwata et al. does not disclose a Flash memory with a copy back command or operation or modified copy back command or operation or control circuits for managing the same. As noted by the Examiner, Iwata et al. also does not teach masking the read data. *See, e.g.*, Iwata et al., Figures 1, 4 and 5; Paragraphs [0016]-[0079] and [0111]-[0142]. Applicant thus submits that Iwata et al. does not teach or suggest a split or a non-split data move circuit or method utilizing a modified copy back operation in a non-volatile memory. As such, Applicant submits that Iwata et al does not teach or suggest each and every element of the Applicant's claimed invention.

Applicant respectfully maintains that Harper, III et al. discloses a memory system for dynamic address mapping for vector access in a memory system and not a non-volatile memory system. Applicant also submits that Harper III, et al. does not disclose masking of data sectors read from the memory or masking of data in a modified copy back operation, but the masking of

a row address field. *See, e.g.*, Harper, III et al., Figure 1; Column 14, lines 38-47; Abstract. Applicant thus submits that Harper, III et al. does not teach or suggest a split or a non-split data move circuit or method utilizing a modified copy back operation in a non-volatile memory. As such, Applicant submits that Harper, III et al. does not teach or suggest each and every element of the Applicant's claimed invention.

Applicant respectfully maintains that Gonzales et al. discloses a non-volatile memory that operates to store variable data sizes and fields in each page of an erase block in order to more efficiently utilize the available memory storage. In this, Gonzales et al. discloses storing in a single page the associated overhead areas for user data areas store in two or more other pages or dividing a user data area and its associated overhead at a randomly selected point and storing them split across two pages. *See, e.g.*, Gonzales et al., Figures 2-9; Summary; Column 9, line 1 to Column 10, line 30. Applicant therefore maintains that Gonzales et al. does not teach or suggest storing user data sectors or areas in two or more physical row pages, such that a first set of user data sectors are stored in a first physical row page along with the associated overhead data areas of a second set of user data sectors, and the associated overhead data areas of the first set of user data sectors are stored in a second physical row page along with the user data areas of the second set of user data sections (or a third set of user data sectors). Applicant also maintains that Gonzales et al. does not teach or suggest a split data non-volatile memory devices or systems as having split user/overhead data that avoids the issue of potential corruption of both the user data and overhead data due to each being held within close proximity to each other or on the same physical row (wordline), or super blocks as pairs of erase blocks where when user data is read from a sector of an erase block of the Flash memory, the overhead data for the user data is read from the overhead data area of a sector of the associated erase block of the erase block super block pair. *See*, Paragraphs [0010], [0025], [0035] and [0038] of the Specification of the Present Application. Applicant therefore maintains that Gonzales et al. does not teach or suggest the split data storage or a split or a non-split data move circuit or method of the claimed invention. As such, Applicant submits that Gonzales et al. does not teach or suggest each and every element of the Applicant's claimed invention.

Applicant respectfully maintains that Miura et al. discloses evaluating an ECC for data as it is transferred from a Flash memory to a DRAM device and not evaluating an ECC for user data as it is moved only within a Flash memory device itself or within a non-volatile memory system. *See, e.g.*, Miura et al., Paragraphs [0110]-[0114]. Applicant thus submits that Miura et al. does not teach or suggest evaluating an ECC for user data as it is moved within the Flash

memory device or system or a split or a non-split data move circuit or method. As such, Applicant submits that Miura et al. does not teach or suggest each and every element of the Applicant's claimed invention.

Applicant thus submits that Estakhri et al., Iwata et al., and Harper, III et al. fail to teach or suggest such a split or a non-split data move circuit or method, either alone or in combination. Applicant also submits that Estakhri et al., Iwata et al., Harper, III et al., and Miura et al. fail to teach or suggest such a split or a non-split data move circuit and method, either alone or in combination.

Applicant submits Estakhri et al., Iwata et al., and Gonzales et al. fail to teach or suggest such a split or a non-split data move circuit or method, either alone or in combination. Applicant also submits Estakhri et al., Iwata et al., Gonzales et al., and Miura et al. fail to teach or suggest such a split or a non-split data move circuit or method, either alone or in combination.

As such, Applicant therefore submits that Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al. fail to teach or suggest all elements of Applicant's claimed invention.

Applicant's independent claims 1 and 85 recite, in part, a non-split data move control circuit is adapted to move one or more selected user data sectors and associated overhead data areas stored in one or more physical row pages of a selected source erase block to a target erase block in a modified copy-back move operation such that selected user data sectors and the associated overhead data areas stored in a source physical row page of the source erase block are moved to a target physical row page of the target erase block by reading the selected user data sectors and the associated overhead data areas into an internal latch of the at least one non-volatile memory device, transferring one or more latched user data sectors and associated overhead data areas from the at least one non-volatile memory device, masking the selected user data sectors and the associated overhead data areas, and writing the selected user data sectors and the associated overhead data areas to the target physical row page. Applicant submits Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al., as detailed above, do not teach or suggest a split or a non-split data move circuit or method utilizing a modified copy back operation in a non-volatile memory, either alone or in combination. As such, Applicant submits that Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al. do not teach or suggest each and every element of claims 1 and 85.

Applicant's independent claims 8, 16, 25, 36, 45, 54, 89, and 102 recite, in part, a split data move control circuit is adapted to move one or more selected user data sectors stored in two

or more physical row pages of a selected source super block to a target super block such that the selected user data sectors stored in a first source physical row page of the source super block are moved to a first target physical row page of the target super block and the associated overhead data areas of the selected user data sectors stored in a second source physical row page of the source super block are moved to a second target physical row page of the target super block. Applicant submits Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al., as detailed above, do not teach or suggest a split data move circuit adapted to move one or more selected user data sectors stored in two or more physical row pages of a selected source super block to a target super block, either alone or in combination. As such, Applicant submits that Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al. do not teach or suggest each and every element of claims 8, 16, 25, 36, 45, 54, 89, and 102.

Applicant's independent claims 29, 44, 46, and 101 recite, in part, a non-split data move control circuit, wherein the non-split data move control circuit is adapted to move one or more selected user data sectors and associated overhead data areas stored in one or more physical row pages of a selected source erase block of the one or more non-volatile memory devices such that the selected user data sectors and the associated overhead data areas stored in a source physical row page of the source erase block are moved to a target physical row page of a target erase block by reading the selected user data sectors and the associated overhead data areas into an internal latch of the one or more non-volatile memory devices, transferring one or more latched user data sectors and associated overhead data areas from the at least one non-volatile memory device, masking the selected user data sectors and the associated overhead data areas, and writing the selected user data sectors and the associated overhead data areas to the target physical row page. Applicant submits Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al., as detailed above, do not teach or suggest a non-split data move circuit adapted to move one or more selected user data sectors and associated overhead data areas by reading the selected user data sectors and the associated overhead data areas into an internal latch of the one or more non-volatile memory devices, transferring one or more latched user data sectors and associated overhead data areas from the at least one non-volatile memory device, masking the selected user data sectors and the associated overhead data areas, and writing the selected user data sectors and the associated overhead data areas to the target physical row page, either alone or in combination. As such, Applicant submits that Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al. do not teach or suggest each and every element of claims 29, 44, 46, and 101.

Applicant's independent claims 69, 75, 84 and 93 recite, in part, reading data of a physical page row of a first source erase block of a source super block from a selected non-volatile memory device of one or more non-volatile memory devices; masking off a first selected range of data column bit values; writing the first selected range of data column bit values to a physical page row of a first target erase block of a target super block; reading data of a physical page row of a second source erase block of the source super block; masking off a second selected range of data column bit values; and writing the second selected range of data column bit values to a physical page row of a second target erase block of the target super block. Applicant submits Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al., as detailed above, do not teach or suggest a method of moving data in super block, either alone or in combination. As such, Applicant submits that Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al. do not teach or suggest each and every element of claims 69, 75, 84 and 93.

Applicant respectfully contends that claims 1, 8, 16, 25, 29, 36, 44, 45, 69, 75, 84, 85, 89, 93, 101 and 102, as pending, have been shown to be patentably distinct from the cited references of Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al., either alone or in combination. As claims 2-7, 9, 11-15, 17, 19-21, 26-27, 30-33, 38-41, 67, 70, 73-74, 76, 78-79, 86-88, 90-92, 94-95 and 98 depend from and further define claims 1, 8, 16, 25, 29, 36, 45, 69, 75, 85, 89, and 93, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1-9, 11-17, 19-21, 25-27, 29-33, 36, 38-41, 44-45, 67, 69-70, 73-76, 78-79, 84-95, 98 and 101-102.

Claims 63-64, 68 and 83 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwata et al. (U.S. Published Application No. 2004/0193774) in view of Harper III, et al. (U.S. Patent No. 4,918,600). Applicant respectfully traverses these rejections and submits that claims 63-64, 68 and 83, as pending, are allowable for at least the following reasons.

Applicant respectfully maintains, as stated above, that Iwata et al. discloses a Flash memory card that has a Flash controller with an erase block data merge circuit which operates to consolidate data to a new erase block from an old erase block and subsequent erasure of the old erase block. Applicant maintains that, in disclosing a data merge circuit and operation, Iwata et al. does not disclose a copy back operation or modified copy back operation in a Flash memory or control circuits for managing the same. As noted by the Examiner, Iwata et al. also does not

teach masking the read data. *See, e.g.*, Iwata et al., Figures 1, 4 and 5; Paragraphs [0016]-[0079] and [0111]-[0142]. In addition, as also stated above, Applicant respectfully maintains that Harper, III et al. discloses a memory system for dynamic address mapping for vector access and not a non-volatile memory system or masking a data move between erase blocks utilizing a modified copy back operation. Applicant also submits that Harper III, et al. does not disclose masking of data sectors read from the memory, but the masking of a row address field. *See, e.g.*, Harper, III et al., Figure 1; Column 14, lines 38-47; Abstract.

Applicant's independent claims 63 and 83 recite, in part, reading data of a physical page row of a source erase block from a selected non-volatile memory device of one or more non-volatile memory devices; transferring selected data from the selected non-volatile memory device; masking off a first selected range of data column bit values; and writing the first selected range of data column bit values to a physical page row of a target erase block.

Applicant submits that Iwada et al. and Harper, III et al., as detailed above, do not teach or suggest a split or a non-split data move circuit or method utilizing a modified copy back operation in a non-volatile memory, either alone or in combination. As such, Applicant submits that Iwada et al. and Harper, III et al. do not teach or suggest each and every element of claims 63 and 83.

Applicant respectfully contends that claims 63 and 83, as pending, have been shown to be patentably distinct from the cited references, either alone or in combination. As claims 64 and 68 depend from and further define claim 63, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 63-64, 68 and 83.

Allowable Subject Matter

Claims 46-62 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 1st paragraph, set forth in this Office action. Applicant thanks the Examiner for this indication. However, as detailed above, claims 46-62 have been shown to be are supported by the specification and that the specification does clearly describe the invention in a way to enable one skilled in the art to make or use the invention. Applicant thus respectfully requests reconsideration and withdrawal of the objection, and allowance of claims 46-62.

Claims 10, 18, 22-24, 28, 34-35, 37, 42-43, 65-67, 71-72, 77, 80-82, 96-97 and 99-100 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any

intervening claims. Applicant also thanks the Examiner for this indication. However, as detailed above, claims 1, 16, 25, 29, 36, 63, 69, 75, and 93 have been shown to be patentably distinct from the cited references. As claims 10, 18, 22-24, 28, 34-35, 37, 42-43, 65-67, 71-72, 77, 80-82, 96-97 and 99-100, depend from and further define claims 1, 16, 25, 29, 36, 63, 69, 75, and 93, they are also deemed to be allowable. Applicant thus respectfully requests reconsideration and withdrawal of the objection, and allowance of claims 10, 18, 22-24, 28, 34-35, 37, 42-43, 65-67, 71-72, 77, 80-82, 96-97 and 99-100.

CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

Date: 10/25/06

Andrew C. Walseth
Reg. No. 43,234

Attorneys for Applicant
Leffert Jay & Polglaze
P.O. Box 581009
Minneapolis, MN 55458-1009
T (612) 312-2200
F (612) 312-2250